CLAIMS:

1. An electronic device (10), comprising:

a data communication bus (12) having a plurality of substantially parallel conductors (12a, 12b, 12c, 12d), the plurality of substantially parallel conductors (12a, 12b, 12c, 12d) comprising a first conductor (12a) and a second conductor (12b); and

a control circuit (14) for providing the first conductor (12a) with a first electrical signal and the second conductor (12b) with a second electrical signal;

characterized by further comprising:

a first signal transition dependent delay circuit (16a) coupled to the first conductor (12a) for delaying a first electrical signal transition; and

a second signal transition dependent delay circuit (16b) coupled to the second conductor (12b) for delaying a second electrical signal transition.

2. An electronic device (10) as claimed in claim 1, characterized in that the first signal transition dependent delay circuit (16a) comprises a logic element (30; 40) having:

a first input (32; 42) being coupled to an input (31) of the first signal transition dependent delay circuit (16a) via a first input delay element (36);

a second input (34; 44) being coupled to the input (31) of the first signal transition dependent delay circuit (16a); and

an output (37; 47) being coupled to the first conductor (12a).

3. An electronic device (10) as claimed in claim 2, characterized in that:

the logic element (30; 40) comprises an AND gate (30); and

the first input delay element (36) comprises an inverter chain having an even number of inverters.

4. An electronic device (10) as claimed in claim 2, characterized by:

the logic element (30; 40) comprising a NOR gate (40);

the first input delay element (36) comprising an inverter chain having an even number of inverters; the first input (42) and the second input (44) of the logic element (40)

being coupled to the input (31) of the first signal transition dependent delay circuit (16a) via an inverter (38).

5. An electronic device (10) as claimed in claim 1, characterized in that the first signal transition dependent delay circuit (16a) comprises an asymmetric inverter (50) having:

an input (31) coupled to the control circuit (14);

an output (57) coupled to the first conductor (12a);

a first transistor (52) having a first resistance; and

a second transistor (54) having a second resistance.

6. An electronic device (10) as claimed in claim 5, characterized by the output (57) of the asymmetric inverter (50) being coupled to the first conductor (12a) via a capacitor (56) and a buffer circuit (58).

7. An electronic device (10) as claimed in claim 1, characterized in that the first signal transition dependent delay circuit (16a) and the second signal transition dependent delay circuit (16b) are integrated in the control circuit (14).